Customer No.: 31561
Docket No.: 12978-US-PA
Application No.: 10/710,420

## REMARKS

### Present Status of Application

Claims 1-5 remain pending in the application. The Final Office Action mailed on June 5, 2006 objected to the specification and claim 1 because the feature "impossible to be used" is not clearly described. The Final Office Action also rejected claims 1-5. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Rich et al. (US Pub. No. 2003/0125917, "Rich" hereinafter). Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rich in view of Rupp et al. (US Patent No. 6,857,110, "Rupp" hereinafter).

The specification, claim 1 and claim 3 have been amended. Applicant believes that these changes do not introduce new matter and reconsideration of claims 1-5 is respectfully requested. In view of the above amendments and the following discussions, a notice of allowance is respectfully solicited.

### Discussion for Minor Amendments

To describe the subject matter more clearly and correctly, Applicant has removed "and" from the sentence "... by referring to a state data contained in a design description and associated to the cell description when ..." in claim 1.

**Discussion for Objections**

The Final Office Action stated that the feature "impossible to be used" is not clearly described and therefore objected to the specification and claim 1. On the contrary, Applicant believes that the feature "impossible to be used" is sufficiently described in the specifications.

According to paragraphs 18 and 19 of the specification, the so-called state-dependent description is the delay data of the I/O path description associated to different input status of a cell. For a cell with multiple input terminals, each input terminal may have different logic states, such as logic 0 or logic 1. The 0/1 combinations of the input terminals are the input states of the cell. By referring to a design description of the IC, for example, by referring to a netlist, it can be known that which states will appear during normal operation conditions defined by the design specifications of the IC and which states will not appear during such normal operation conditions. The latter states will not be used by the simulator. Therefore delay descriptions associated with the latter states are **impossible to be used**, or not intended to be used, and can be safely removed to reduce SDF file sizes.

Anyone skilled in the art can easily deduce the meaning of "impossible to be used" from the disclosure of paragraphs 18 and 19 of the specification as shown above. To further clarify this concept, Applicant has replaced the phrase "impossible to be used" in

the specification and the claims with "not intended to be used". Applicant believes that this amendment does not introduce new matter.

**Discussion for 35 U.S.C. 102(b) Rejections**

The Final Office Action rejected claim 1 as being anticipated by Rich. Applicant respectfully disagrees. Claim 1 is patentable for at least the reasons below.

Although claim 1 and Rich both focus on reducing SDF file sizes, they use different approaches.

**Claim 1 reduces SDF file sizes by removing state-dependent descriptions which are not intended to be used.** According to paragraphs 18 and 19 of the specification, the state-dependent descriptions removed in claim 1 are descriptions associated with the states which will not appear during normal operation conditions of an IC. The states of a cell are the logic 0/1 combinations of the input terminals of the cell.

On the other hand, according to Rich's paragraph 12, Rich's approach select delay values from a VHDL standard delay file that correspond to an instance of a logic gate in a logic model. Then the system collects all the delay values of the selected instance and builds super generics for the rise-time and the fall-time of the selected instance. Then, the system repeats this process for every delay value in the standard delay file that correspond to every instance of every logic gate in the logic model. The system then outputs a

reduced size standard delay file containing the super generics for every instance of every logic gate in the logic model. According to Rich's paragraph 100, Rich can reduce SDF file size because each super generic is represented by a collection of pointers into a data structure containing all the relevant delay values. For each instance, the collection of pointers, that point into the data structure for the super generic to be able to resolve the actual delay values for the particular instance, takes up significantly much less storage than a set of conventional generics.

The only removal performed by Rich is at step 607 in Fig. 6. According to paragraph 54 of Rich, all the delays assigned to a generic for the entire chip are extracted from the values in the SDF file. The delays are sorted and any duplicate delay entries are removed. Then the sorted delays are grouped into sets of up to 62 entries corresponding to correlation sets.

Comparing claim 1 and Rich, it can be easily seen that many limitations in claim 1 are absent from Rich's teachings.

Rich does not tech the second step of claim 1, "determining whether or not a state-dependent description is present in the cell description", because Rich does not tech state-dependent descriptions. As mentioned above, state-dependent descriptions are delay descriptions associated with the logic states of input terminals of a cell. Although Rich discloses logic gates with multiple input terminals, Rich does not consider logic

state combinations of the input terminals of each cell.

Rich does not tech the third step of claim 1, "removing the state-dependent descriptions in the cell description, which are not intended to be used, by referring to a state data contained in a design description associated to the cell description when it is determined that the state-dependent description is present in the cell description". Rich does not teach the "state" as recited in claim 1. Consequently, it is impossible for Rich to teach the "state data contained in the design description". It is also impossible for Rich to teach "state-dependent descriptions". It follows that Rich does not teach "state-dependent descriptions which are not intended to be used". And Rich's approach cannot make decisions based on whether "the state-dependent description is present in the cell description".

Rich removes only duplicate delay entries, which are absolutely different from the state-dependent descriptions removed in claim 1. State-dependent descriptions not intended to be used do not have to be duplicate, since they may appear only once in an SDF file. From another point of view, duplicate delay entries may all be used by the simulator because they may belong to different gate instances on frequently used transmission paths. Rich teaches nothing about the possibility of delay entries to be used. Rich simply removes and correlate delay entries regardless of their state dependency and possibility to be used.

In Response to Applicant Remarks, the Final Office Action stated that paragraph 7 of the application states: "the delay data of each I/O path contains four state-dependent descriptions", which corresponds to one or more of "delay entries", "delay values", and "delay data" in Rich. Applicant respectfully disagrees. For reasons shown above, the **generic** delay entries in Rich cannot be equated with the **state-dependent** delay descriptions in claim 1.

In Response to Applicant Remarks, the Final Office Action enumerated four features (A-D) in Rich corresponding to the "impossible to be used" (now "not intended to be used") limitation in claim 1. Applicant respectfully disagrees. The reasons are listed below.

In regard to features A and C, although claim 1 and Rich have similar purposes, that is, reducing SDF file sizes, the conclusion that the limitations of claim 1 are disclosed by Rich should not be reached through hindsight merely because claim 1 and Rich have similar purposes. As mentioned above, the steps taken by claim 1 and Rich to reduce SDF file sizes are patently distinguishable.

In regard to feature B, "duplicated delay is impossible to be used, i.e., redundancy", the duplicate entries in Rich is not equivalent to the delay descriptions removed in claim 1. Claim 1 removes redundant **state-dependent** delay descriptions, which have to be determined by referring to the design description of the IC (paragraphs

18 and 19). In comparison, Rich teaches neither input state nor state dependency.

In regard to feature D, Applicant believes that it is irrelevant to the anticipation of claim 1 by Rich.

For at least the reasons above, Applicant believes claim 1 is patently distinguishable from Rich and is allowable. Since claims 2-4 depend on independent claim 1, each of claims 2-4 includes all limitations of claim 1. Consequently, claims 2-4 are also patently distinguishable from Rich and are allowable.

**Discussion for 35 U.S.C. 103(a) rejections**

The Final Office Action rejected claim 5 as being unpatentable over Rich in view of Rupp. Applicant respectfully disagrees. Claim 5 is patentable for at least the reasons below.

Based on the discussion for 35 U.S.C. 102(b) rejections above, Applicant believes that Rich does not teach all limitations of claim 1. Claim 5 depends on claim 1 and includes all limitations of claim 1. Therefore, adding Rupp's SDF IEEE 1497 into Rich does not help to render claim 5 obvious. Claim 5 is patentable over Rich in view of Rupp.

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## CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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